REMARKS

In the Office Action dated September 29, 2003, the Examiner has ***finally rejected*** claims 3, 4, 9, and 12-14 pending in the application on the basis of new ground(s) of rejection and newly cited art. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated September 29, 2003.

A good and sufficient reason why the present response is necessary and was not earlier presented is that an entirely new reference has been cited in the present final rejection dated September 29, 2003 (37 CFR §1.116(c)). The new reference is Juang et al. (USPN 5,547,882) (hereinafter "Juang"), which is for the first time brought to Applicant's attention by means of the present ***final rejection*** dated September 29, 2003. The new reference, i.e. Juang, was not cited in the present application prior to the instant final rejection. Since Juang is a reference upon which the Examiner has now relied, Applicant believes that it would be manifestly unfair for the Patent Office not to consider Applicant's arguments, which are necessitated due to the newly cited reference, Juang.

The Examiner has rejected claims 3, 4, 9, and 12-14 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,894,146 to Pio et al. ("Pio") in view of Juang. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 3 and 9, is patentably distinguishable over Pio and Juang, singly or in combination.

The present invention, as defined by independent claims 3 and 9, teaches, among other things, source and drain regions and a channel region formed in a well and a dopant

concentration region displaced about a target region situated below the channel region, where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. As disclosed in the present application, the present invention provides a retrograde dopant distribution in the channel region between source and drain regions of a floating gate transistor. As disclosed in the present application, the dopant distribution increases from the level in the substrate closest to the tunnel oxide to the level of the target area and then decreases down through the substrate. Additionally, as disclosed in the present application, the dopant distribution has a highest concentration level toward a centerline axis around the target area and decreases laterally toward opposing source and drain regions. As a result, the present invention advantageously achieves reduced series resistance of series-connected floating gate transistors, which allows a desired reduction in source/drain dopant levels in order to combat undesirable short channel effects.

In contrast to the present invention as defined by independent claims 3 and 9, Pio and Juang do not teach, disclose, or suggest source and drain regions and a channel region formed in a well and a dopant concentration region displaced about a target region situated below the channel region, where the well has a first conductivity type and the source and drain regions and the dopant concentration region have a second conductivity type. Pio specifically discloses floating gate transistor 2, selection transistor 3, source region 15, and drain region 16, where floating gate transistor 2 is connected in series with selection transistor 3. See, for example, column 5, lines 51-56 and Figure 8 of Pio.

However, Pio fails to teach, disclose, or suggest a dopant concentration region displaced about a target region situated below a channel region of a floating gate transistor.

Pio discloses providing a double implant of arsenic and phosphorus in region (e) between respective gates of transistors 1 and 2 for the purpose of reducing the so-called band-to-band current. See, for example, column 4, lines 60-65 and Figures 1 and 6 of Pio. However, Pio does not mention undesirable short channel effects or provide any motivation for forming a retrograde dopant concentration profile in the channel region of a floating gate transistor.

Juang specifically discloses gate 62 situated on gate oxide layer 50, which is formed on silicon substrate 30, and LDD (Lightly Doped Drain) regions 64, which are formed by implanting phosphorus ions in silicon substrate 30 adjacent to gate 62. See, for example, column 2, lines 53-65 and Figures 5 and 6 of Juang. In Juang, a retrograde channel profile is accomplished by implanting phosphorus ions through gate 62 into channel 66 to obtain proper threshold voltage. See, for example, column 3, lines 2-6 and Figure 6 of Juang. However, Juang fails to teach, disclose, or suggest a dopant concentration displaced about a target region, where the target region is situated below the channel region, and where the dopant concentration region extends into the channel region such that the channel region has a non-uniform concentration of dopant.

In Juang, the retrograde channel profile determines channel profile curve 73, which shows a retrograde dopant distribution in channel 66. See, for example, column 3, lines 18-28 and Figure 7 of Juang. However, Juang fails to teach, disclose, or suggest a

dopant concentration region displaced about a target region, where the dopant concentration region has a highest concentration level toward a centerline axis around the target area and decreases laterally toward opposing source and drain regions.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 3 and 9, is not suggested, disclosed, or taught by Pio and Juang, either singly or in combination thereof. As such, the present invention, as defined by independent claims 3 and 9, is patentably distinguishable over Pio and Juang. Thus claim 4 depending from independent claim 3 and claims 12-14 depending from independent claim 9 are, *a fortiori*, also patentably distinguishable over Pio and Juang for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by independent claims 3 and 9 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 3, 4, 9, and 12-14 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 3, 4, 9, and 12-14 pending in the present application is respectfully requested.

Respectfully Submitted,
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